

使用 HT82A525R 实现与 PC 的数据传输

文件编码: HA0270S

简介

HT82A525R 具有 USB 功能, 提供 4 个端点 (Endpoint), 可支持传输分别有控制型 (Control Mode)、中断型 (Interrupt Mode) 及巨量型 (Bulk Mode)。FIFO 大小共 208 Bytes, 8、8、64、64*2 对应端点 0~4。

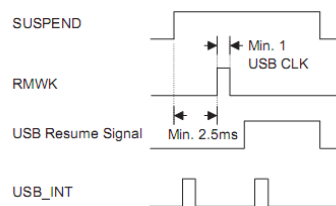
本范例将介绍 HT82A525R 与 PC 的数据传送, 将端点 1 配置为 IN, 端点 2 配置为 OUT, 通过 PC 端的测试软件利用中断传输实现 8 Bytes 数据的输入与输出。

工作原理

跟 USB 相关的寄存器有 12 个, 包括 USC(20H)、USR(21H)、UCC(22H)、AWR(23H)、STALL(24H)、SIES(25H)、MISC(26H)、SETIO(27H)、FIFO0(28H)、FIFO1(29H)、FIFO2(2AH)、FIFO3(2BH)。

USC寄存器的定义

如果在 USB 总线上超过 3ms 没有信号, 设备将进入 Suspend Mode, 此时 USC 寄存器中的 SUSP 位将被置 1, 并产生 USB 中断, 如下图所示。为了减小 Suspend 电流需要清除 UCC 寄存器中的 USBCKEN 位, 为了进一步降低功耗可以通过置位 SUSP2 来实现。当设备接收到主机发送的 Resume 信号时, MCU 会产生中断, 此时我们需要打开 USB 的时钟, 即 USBCKEN=1, 并清除 SUSP2。



HT82A525R 支持 Remote Wake-up 功能, 如果设备配置为具有该功能时, 设备通过控制 RMWK 发送一个 Wake-up 脉冲来唤醒 USB 主机, 如上图所示。

Bit No.	Label	R/W	Function
0	SUSP	R	USB suspend indication flag 0: not in suspend mode 1: in suspend mode When this bit is set to "1" (set by SIE), it indicates that the USB bus enters the suspend mode. The USB interrupt is also triggered on any changes of this bit.
1	RMWK	R/W	USB remote wake-up command 0: disable 1: enable It is set by the MCU to force the USB host leaving the suspend mode. Set RMWK bit to "1" to enable remote wake-up. When this bit is set to "1", a 2 μ s delay for clearing this bit to "0" is needed to insure that the RMWK command is accepted by the SIE.
2	URST	R/W	USB reset indication bit 0: no USB reset 1: USB reset This bit is set or cleared by USB SIE. When the URST is set to "1", this indicates that a USB reset has occurred and a USB interrupt will be initialized.
3	RESUME	R	USB resume indication bit 0: in suspend mode 1: resume When the USB leaves the suspend mode, this bit is set to "1" (set by SIE). This bit will appear for 20ms, waiting for the MCU to detect it. When the RESUME is set by SIE, an interrupt will be generated to wake-up the MCU. In order to detect the suspend state, MCU should set the USBCKEN and SUSP2 (in the SCC register) to enable the SIE detect function. The RESUME will be cleared while the SUSP is set to "0". When MCU detects the SUSP, the RESUME (which causes MCU to wake-up) should be remembered and taken into consideration.
4	V33O	R/W	V33O enable control bit 0: turn off 1: turn on
5	PLL	R/W	PLL enable control bit 0: turn on 1: turn off
6	—	—	Unused bit, read as "0"
7	URD	R/W	USB reset signal control function definition 1: Will reset the MCU 0: Cannot reset the MCU

USC (20H) Definitions

USR寄存器的定义

USR 寄存器用来指示由哪一端点引起的中断，端点请求标志位 (EPOIF、EP1IF、FP2IF 和 EP3IF) 用于指示哪些端点被访问，端点中断使能位 (EEP0I、EEP1I、EEP2I 和 EEP3I) 用于控制端点中断的使能和除能。

Bit No.	Label	R/W	Function
0	EP0IF	R/W	The endpoint 0 interrupt request flag 0: inactive 1: active When this bit is set to "1" (set by SIE), it indicates that the endpoint 0 is accessed and a USB interrupt will occur. When the interrupt has been served, this bit should be cleared by firmware.
1	EP1IF	R/W	The endpoint 1 interrupt request flag 0: inactive 1: active When this bit is set to "1" (set by SIE), it indicates that the endpoint 1 is accessed and a USB interrupt will occur. When the interrupt has been served, this bit should be cleared by firmware.
2	EP2IF	R/W	The endpoint 2 interrupt request flag 0: inactive 1: active When this bit is set to "1" (set by SIE), it indicates that the endpoint 2 is accessed and a USB interrupt will occur. When the interrupt has been served, this bit should be cleared by firmware.
3	EP3IF	R/W	The endpoint 3 interrupt request flag 0: inactive 1: active When this bit is set to "1" (set by SIE), it indicates that the endpoint 3 is accessed and a USB interrupt will occur. When the interrupt has been served, this bit should be cleared by firmware.
4	EEP0I	R/W	The endpoint 0 interrupt enable 0: disable 1: enable
5	EEP1I	R/W	The endpoint 1 interrupt enable 0: disable 1: enable
6	EEP2I	R/W	The endpoint 2 interrupt enable 0: disable 1: enable
7	EEP3I	R/W	The endpoint 3 interrupt enable 0: disable 1: enable

USR (21H) Definitions

UCC寄存器的定义

UCC 寄存器中的 EPS0~EPS2 用于 FIFO 的选择，SYSCLK 用于选择系统时钟采用 6MHz 还是 12MHz，RCTRL 用于选择 VBUS 与 D+ 中间是否有 7.5K 的电阻存在。

Bit No.	Label	R/W	Function
0 1 2	EPS0 EPS1 EPS2	R/W	Accessing endpoint FIFO selection. EPS2, EPS1, EPS0: 000: Select endpoint 0 FIFO 001: Select endpoint 1 FIFO 010: Select endpoint 2 FIFO 011: Select endpoint 3 FIFO 100: Reserved for future expansion, cannot be used 101: Reserved for future expansion, cannot be used 110: Reserved for future expansion, cannot be used 111: Reserved for future expansion, cannot be used If the selected endpoints do not exist, the related functions are not available.
3	USBCKEN	R/W	USB clock Control bit 0: disable 1: enable
4	SUSP2	R/W	Suspend mode control bit 0: Normal Mode 1: HALT Mode This bit is used to reduce power consumption in suspend mode. In normal mode, clear this bit to "0". In HALT mode, set this bit to "1" to reduce power consumption.
5	—	—	Unused bit, read as "0"
6	SYSCLK	R/W	System clock oscillator frequency control bit 0: 12MHz 1: 6MHz This bit is used to specify the system clock oscillator frequency used by the MCU. If a 6MHz crystal oscillator or resonator is used, this bit should be set to "1". If a 12MHz crystal oscillator or resonator is used, this bit should be cleared to "0".
7	RCtrl	R/W	7.5kΩ resistor between USBDP and Vbus select bit 0: without resistor 1: with resistor

UCC (22H) Definitions

AWR寄存器的定义

AWR 寄存器用于控制远程唤醒功能和设置 USB 设备的地址。

Bit No.	Label	R/W	Function
0	WKEN	R/W	Remote wake-up enable/disable 0: disable 1: enable
1~7	AD0~AD6	R/W	USB device address

AWR (23H) Definitions

STALL寄存器的定义

STALL 寄存器用于控制 USB 端点进入 STALL 状态。

Bit No.	Label	R/W	Function
0~3	STL0~STL3	R/W	stalled USB endpoints control
4~7	—	—	Undefined bit, read as "0"

STALL (24H) Definitions

SIES寄存器的定义

Bit No.	Label	R/W	Function
0	Adr_set	R/W	Device address configuration bit 0: update device address immediately 1: update by the IN operation
1	F0_ERR	R/W	accessed FIFO0 errors indication bit 0: no errors 1: some errors This bit is set by the USB SIE and cleared by F/W.
2~6	—	—	Unused bit, read as "0"
7	NMI	R/W	NAK interrupt mask bit 0: not mask 1: mask

SIES Function Table

SETIO寄存器的定义

Bit No.	Label	R/W	Function
0	DATATG*	R/W	Data toggle control bit To toggle this bit, all the DATA token will send a DATA0 first.
1~3	SETIO1~3**	R/W	endpoints input or output pipe selection bit 0: output pipe; 1: input pipe
4~7	—	—	Undefined bit, read as "0"

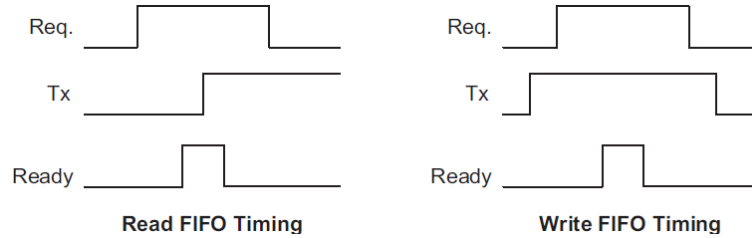
SETIO (27H) Register, USB Endpoint 1~Endpoint3 Set IN/OUT Pipe Register

MISC寄存器的定义

Bit No.	Label	R/W	Function
0	REQUEST	R/W	FIFO request control bit 0: not requested; 1: requested After selecting the desired endpoint, FIFO can be requested by setting this bit as high active. Afterwards, this bit must be set low.
1	TX	R/W	The direction and transition end indication bit 0: read data from FIFO; 1: write data to FIFO This indicates the direction and transition end which the MCU accesses. When set as logic "1", the MCU writes data to FIFO. Afterwards, this bit must be set to logic "0" before terminating request to indicate transition end. For reading action, this bit must be set to logic 0 to indicate that the MCU wants to read and must be set to logic "1" afterwards.
2	CLEAR	R/W	Clear requested FIFO control bit 0: not clear; 1: clear This indicates an MCU clear requested FIFO, even if the FIFO is not ready. After clearing the FIFO, USB interface will send force_tx_err to tell Host that data under-run if Host wants to read data.
3	SDMAEN	R/W	Serial DMA control bit 0: disable; 1: enable This bit is used to control the enable or disable the SBDR of the serial interfaces (which is pin-shared with port E or port C) being written to FIFO3 directly. SPI interfaces can be controlled by MCU and MCU can transmit or receive data by writing or reading SBDR. It is allowed changing from 1 to 0 when the FIFO is not full.
4	SDMASEL	R/W	Serial DMA interface selection bit 0: Serial interface 1 (pin-shared with port E) 1: Serial interface 2 (pin-shared with port C)
5	SETCMD	R/W	FIFO command data indication bit 0: not SETCMD token; 1: SETCMD token
6	READY	R	FIFO ready indication bit 0: not ready to work; 1: ready to work
7	LEN0	R/W	Host sent 0-sized packet indication bit 0: not 0-sized packet; 1: 0-sized packet

MISC (26H) Definitions

在 MISC 寄存器中有几个跟 USB FIFO 读取相关的设置，可分为写入 FIFO 与读取 FIFO 的时序。以下图来说明 FIFO 写入和读取的时序。

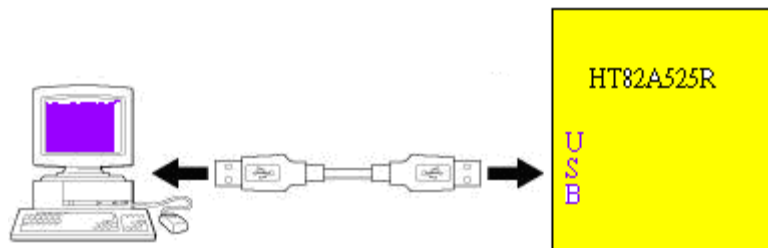


Actions	MISC Setting Flow and Status
Read FIFO0 sequence	00H→01H→delay 2μs, check 41H→read* from FIFO0 register and check not ready (01H)→03H→02H
Write FIFO0 sequence	02H→03H→delay 2μs, check 43H→write* to FIFO0 register and check not ready (03H)→01H→00H
Check whether FIFO0 can be read or not	00H→01H→delay 2μs, check 41H (ready) or 01H (not ready)→00H
Check whether FIFO0 can be written or not	02H→03H→delay 2μs, check 43H (ready) or 03H (not ready)→02H
Write 0-sized packet sequence to FIFO0	02H→03H→delay 2μs, check 43H→01H→00H
Clear FIFO0 sequence	01H→delay 2μs→05H→delay 2μs→00H

Note: *: There are 2μs existing between 2 reading action or between 2 writing → action.

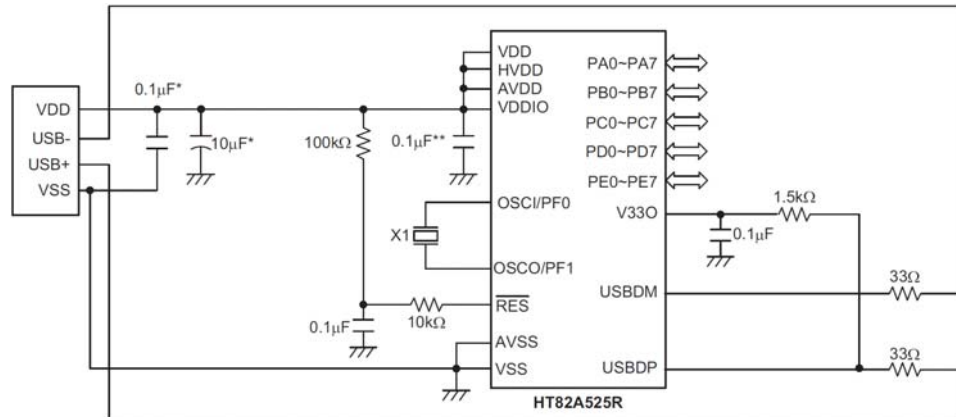
Read or Write FIFO Table

H/W功能方块图



PC 通过 USB 向 HT82A525R 传输 8 Bytes 的数据，HT82A525R 收到数据后，将这笔数据回传给 PC。

应用电路

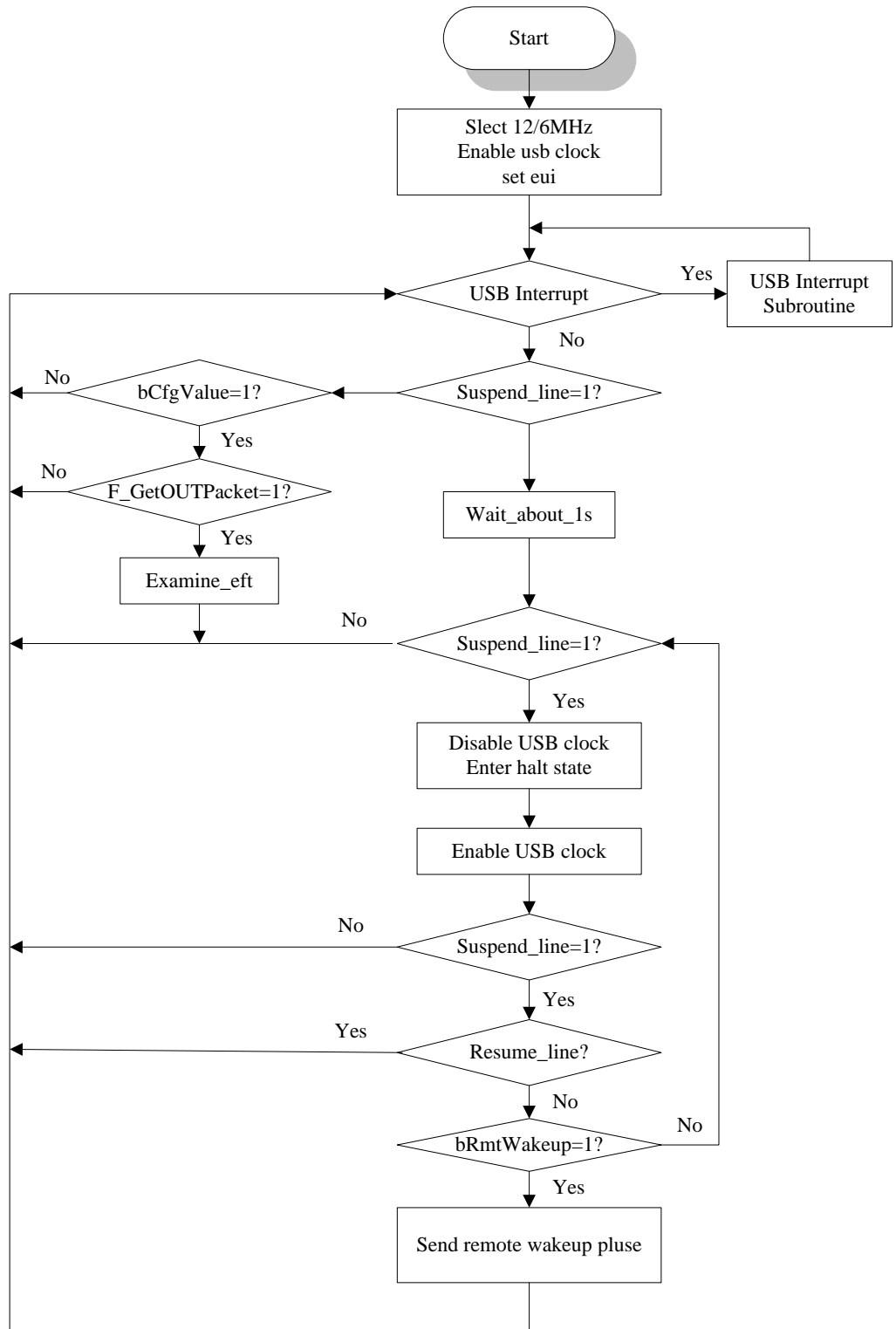


说明:

- 晶振 X1 可以通过寄存器设置选择为 6MHz 或 12MHz, 晶振需尽量靠近 IC 的 OSC1/OSC2 引脚。
- 因为为全速设备, 因此需要在 D+ 和 V330 间接一个 $1.5k\Omega \pm 5\%$ 的上拉电阻。
- USB 2.0 标准规定全速设备, 必须在收发器外部的 D+、D- 引脚上串接电阻, 这是为了正确匹配特定传输线的阻抗。为了匹配这个负载, 全速收发器的输出阻抗必须在 28Ω 到 44Ω 之间, 推荐 D+、D- 引脚上串接的电阻为 33Ω 。
- 带 “*” 符号的电容在 PCB Layout 时需尽量靠近 USB 连接器。
- 带 “**” 符号的电容在 PCB Layout 时需尽量靠近 MCU。

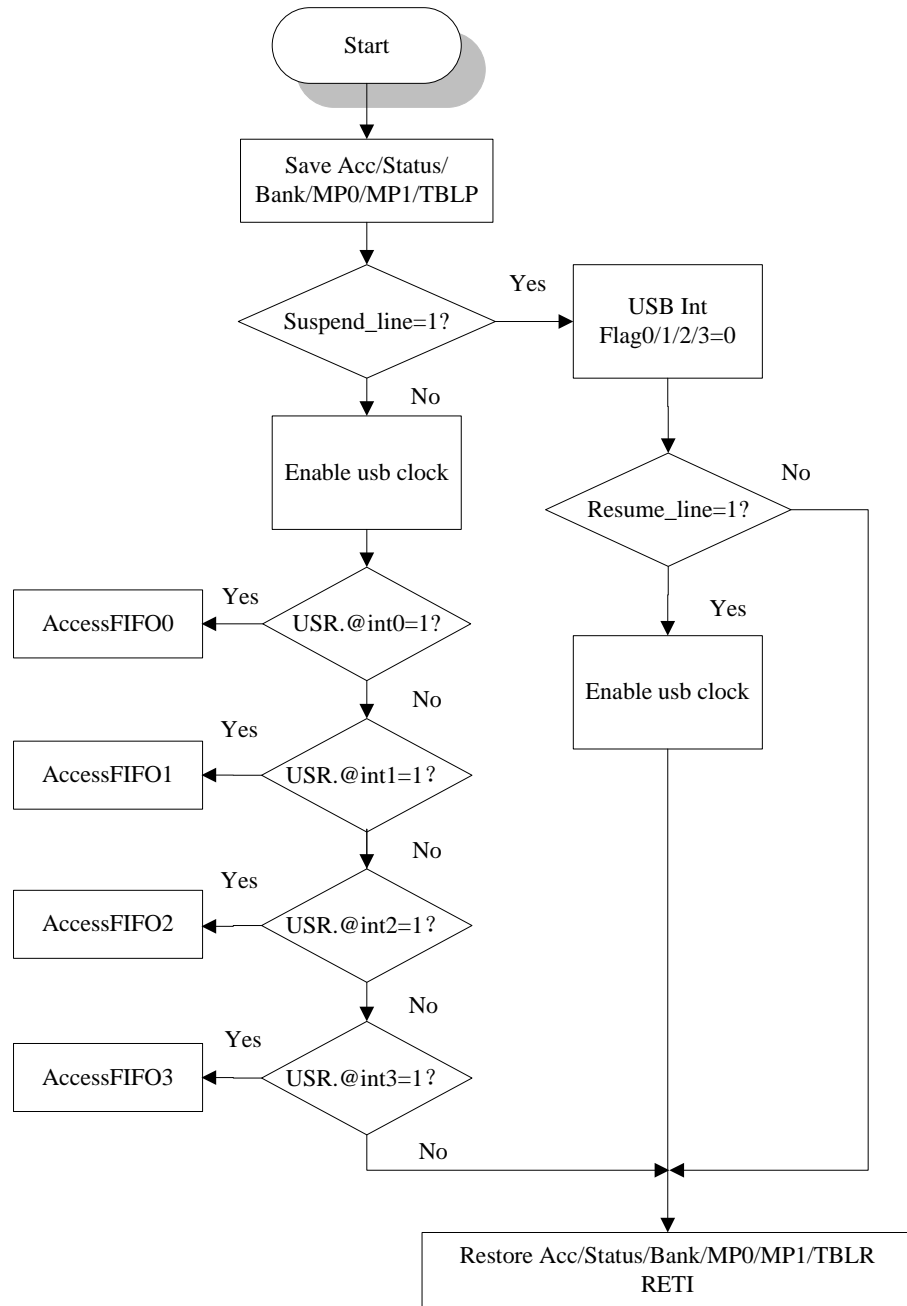
S/W流程图

主流程图



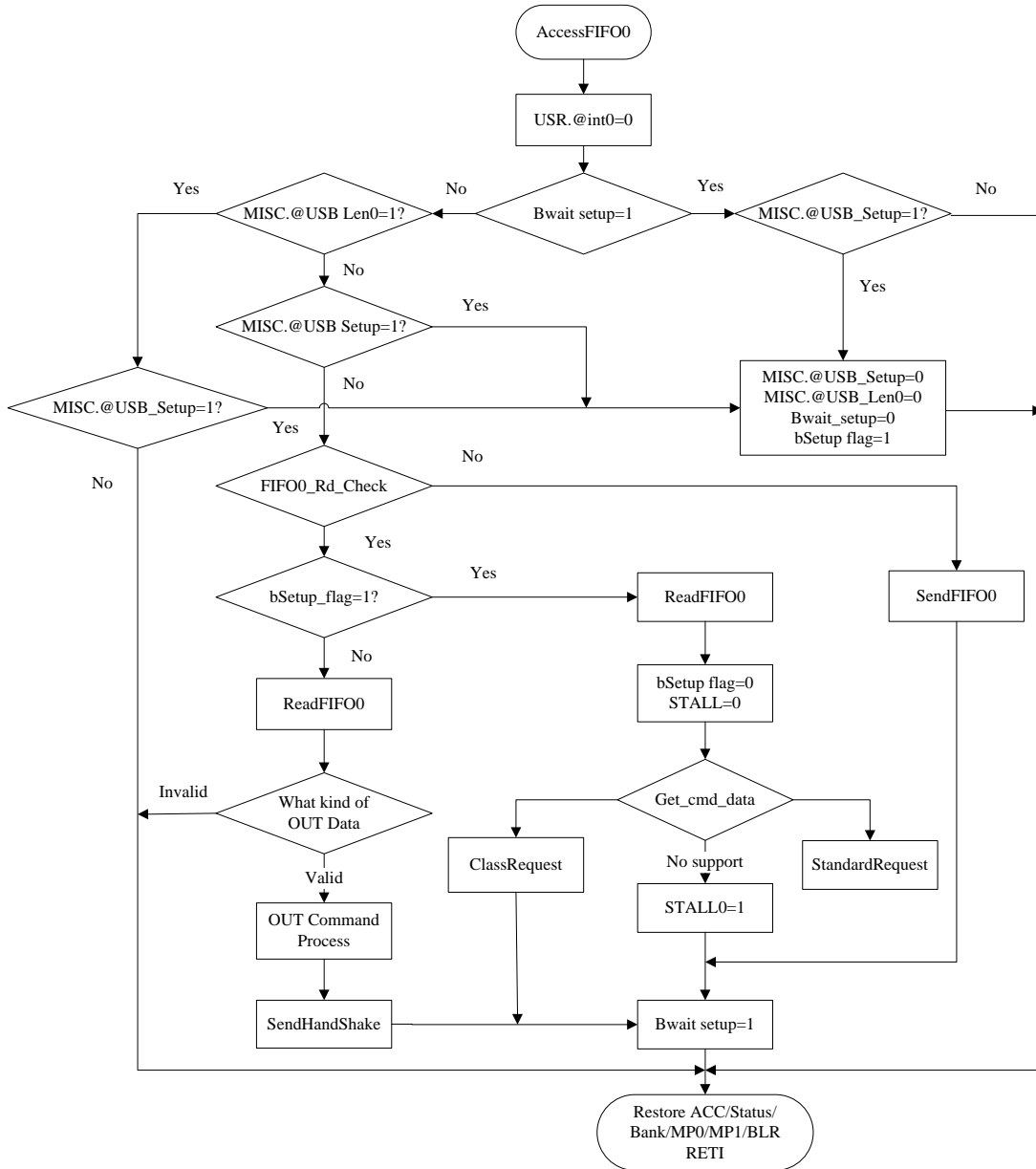
主程序主要是系统的初始化、抗 EFT 及 Suspend 的检测，当有 USB 中断产生时进入 USB 中断子程序；当 USB 进入 Suspend 模式时，MCU 进入 HALT 模式，当有外部中断唤醒 MCU，打开 USB Clock，判断是否允许 Remote Wake-up，如果允许则发送 Remote Wake-up Pulse。

USB中断子程序流程图



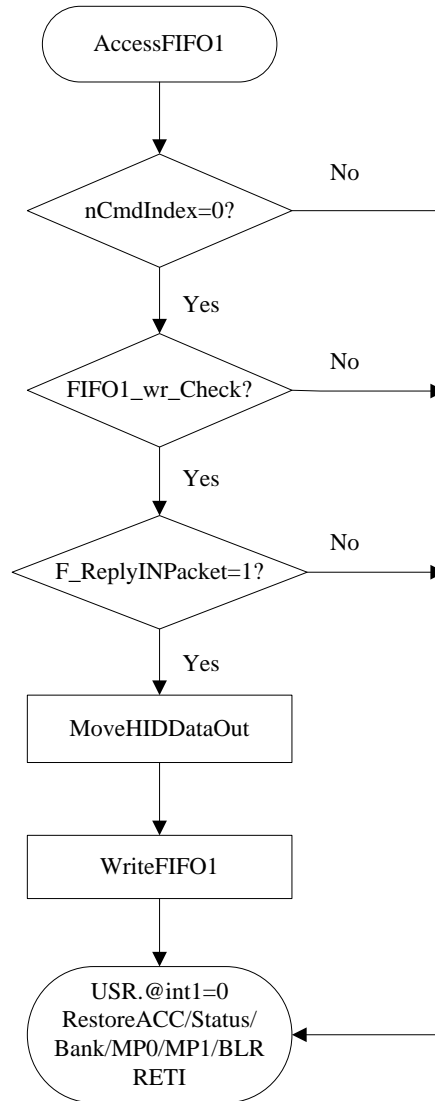
中断子程序主要是判断是 Suspend、Resume 引起的中断还是存取端产生的中断，如果是存取中断端产生的中断，则进入相应的子程序。

存取端点 0 子程序流程图



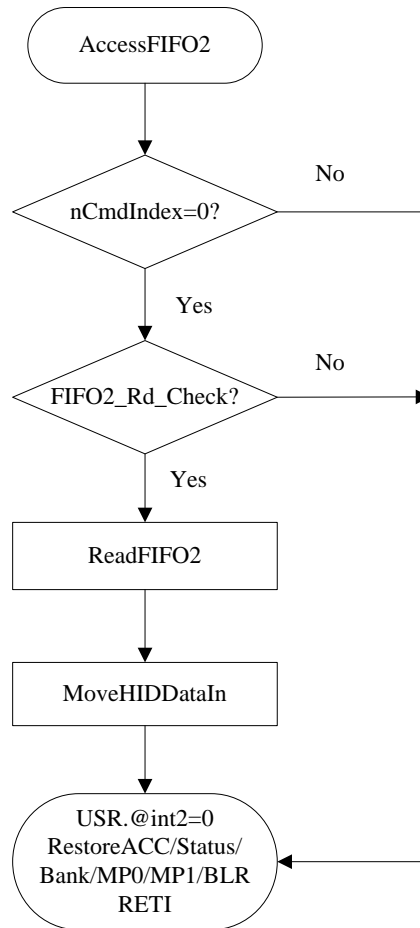
存取端点 0 子程序主要是用于 USB 枚举过程的，首先判断有没有 Setup Token，如果有，将相应标志(bSetup_flag)设为 1，退出中断；如果没有，判断是不是 Len0 包，如果是则退出中断；如果不是 Setup Token 也不是 Len0 包，则先判断 FIFO0 是否可读(IN 或 OUT)，如果可读(OUT)，则读取 FIFO 的数据，若 bSetup_flag=1，代表要处理 Setup Command，再根据命令返回 HOST 所需的数据，若 bSetup_flag 不为 1，代表是一般的 OUT Data；如果 FIFO 可写(IN)，则发送数据。

存取端点 1 子程序流程图



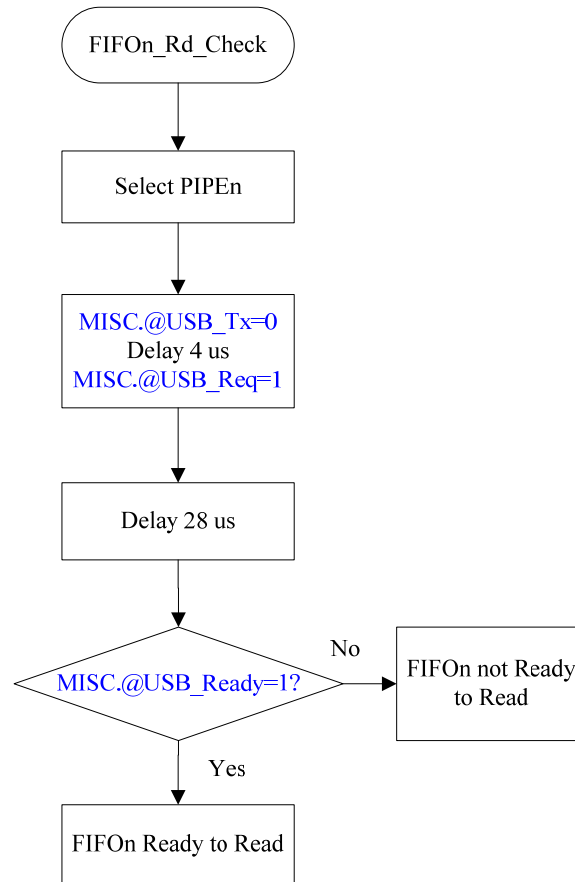
存取端点 1 子程序主要是用来发送 8 Bytes 的数据给 PC。

存取端点 2 子程序流程图

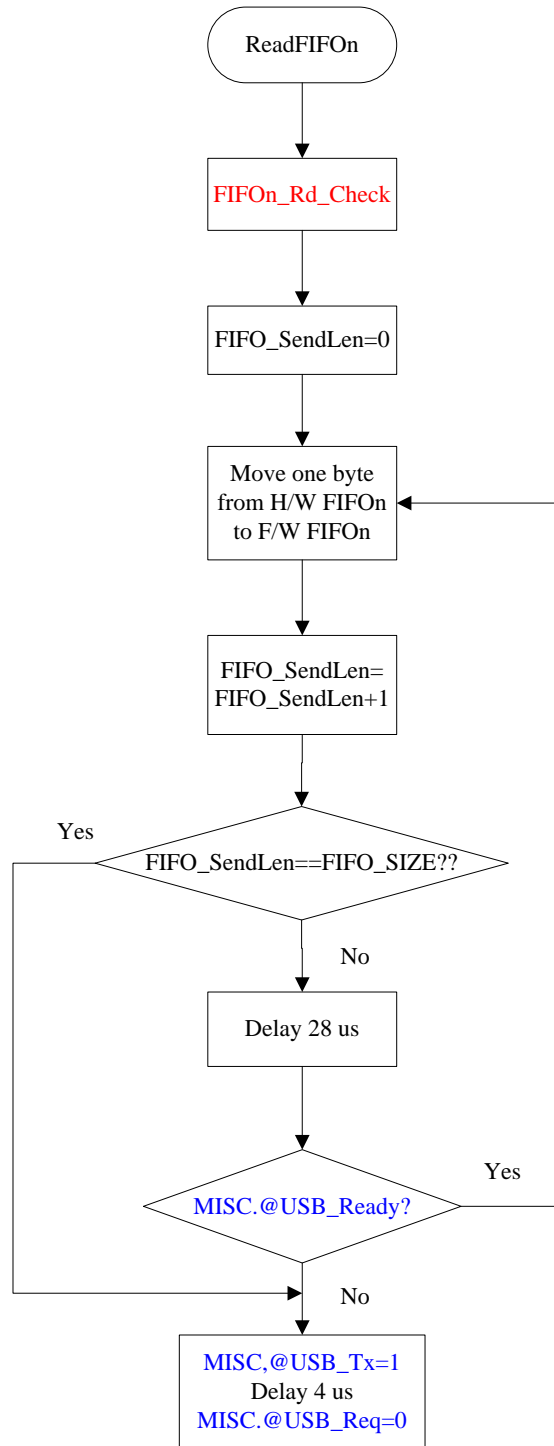


存取端点 2 子程序主要是用来接收 PC 发过来的 8 Bytes 的数据。

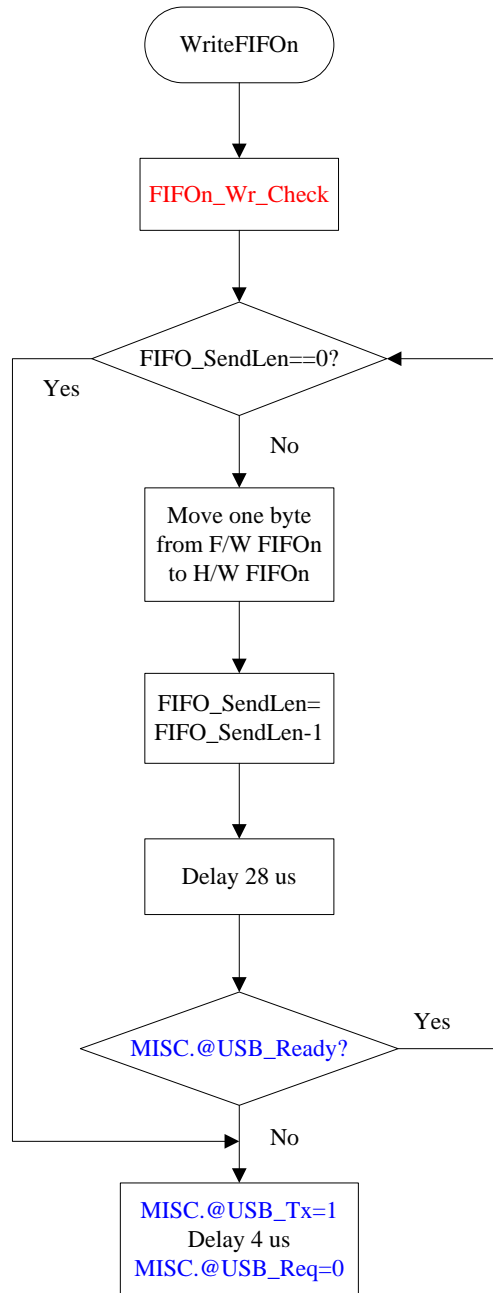
FIFOn_Rd_Check程序流程图



读取FIFO的数据子程序流程图



写FIFO的数据子程序流程图



文件说明

- MAIN.ASM
该 ASM 文件中的内容为主程序，包括寄存器和 I/O 端口的初始化操作等。
- USB_INT.ASM
该 ASM 文件的内容为 USB 的中断服务程序，当发生 USB 中断时，程序会跳到此处。
- USB_LIB.ASM
该 ASM 文件的内容为对 FIFO 进行读、写的子程序。
- STD.ASM
该 ASM 文件的内容为 USB 定义的 11 种标准 USB 请求的子程序。

- CLS.ASM
该 ASM 文件的内容为 HID 设备类请求子程序。
- DES.ASM
该 ASM 文件的内容为所有描述符的定义。
- Variable.ASM
该 ASM 文件中的内容定义了 USB 功能所用到的所有变量。

结论

本文通过介绍如何使用 HT82A525R 的 USB 功能来实现与 PC 端 USB 主机的 8 Bytes 的数据接收与发送。

附件



525R-HID-IN8-OUT8-ASM-NoPCL-12MHz.zip



HT82A525R Test Suite Report.zip

版本记录

版本：V1.10

修改人员：马灵

修改日期：2011 年 12 月 20 日

修改内容：

正文中“UCC 寄存器的定义”小节删除“FSYS16MHz 用于选择系统时钟是使用外部 OSC 还是内部 PPL 16MHz，”。