

Features

- Operating voltage: 2.4V~5.5V
- Multiple LED display – 32 out bits/8 commons and 24 out bits/16 commons
- Integrated display RAM – select 32 out bits & 8 commons for 64×4 display RAM, or select 24 outbits & 16 commons for 96×4 display RAM
- 16-level PWM brightness control
- Integrated 256kHz RC oscillator
- Serial MCU interface – \overline{CS} , \overline{RD} , \overline{WR} , DATA
- Data mode & command mode instruction
- Cascading function for extended applications
- Selectable NMOS open drain output driver and PMOS open drain output driver for commons
- 52-pin QFP package

Applications

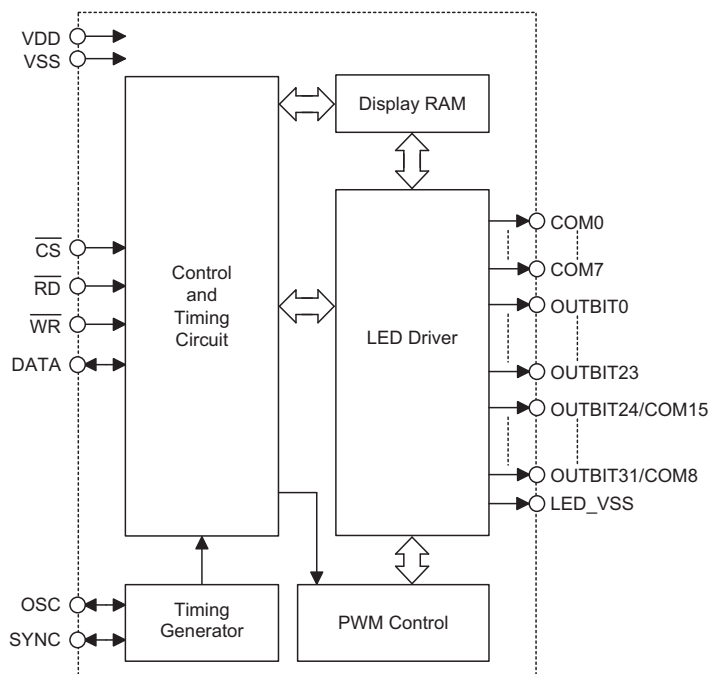
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Other consumer application
- LED Displays

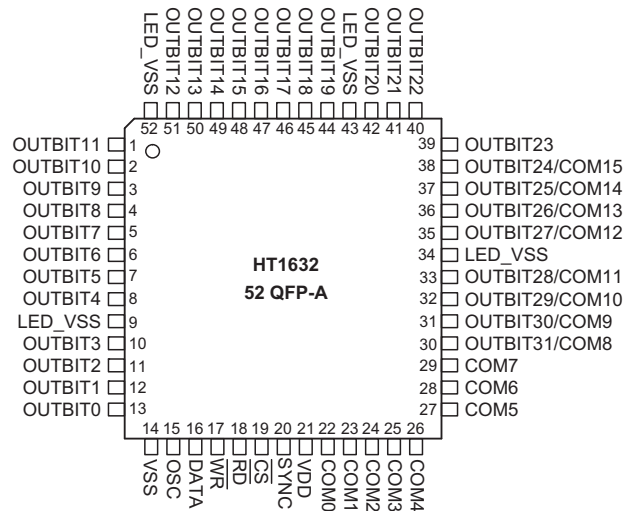
General Description

The HT1632 is a memory mapping LED display controller/driver, which can select a number of out bits and commons. These are 32 out bits & 8 commons and 24 out bits & 16 commons. The device supports 16-gradation LEDs for each out line using PWM control with software instructions. A serial interface is conveniently provided for the

command mode and data mode. Only three or four lines are required for the interface between the host controller and the HT1632. The display can be extended by cascading the HT1632 for wider applications.

Block Diagram



Pin Assignment

Pin Description

Pad Name	I/O	Description
OUTBIT0~OUTBIT23	O	Line drivers. These pins drive the LEDs.
OUTBIT24/COM15~ OUTBIT31/COM8	O	Drive LED output or Common output
COM0~COM7	O	Common outputs
SYNC	I/O	If the MASTER MODE command is programmed, the synchronous signal is output to SYN pin. If the SLAVE MODE command is programmed, the synchronous signal is input from SYN pin.
OSC	I/O	If the system clock is sourced from an external clock source, the external clock source should be connected to this pad. If the on-chip RC oscillator is selected, this pad can be connected to a high or low level. If the cascade mode is selected, this pad is the driver clock signal.
DATA	I/O	Serial data input or output with pull-high resistor
\overline{WR}	I	WRITE clock input with pull-high resistor Data on the DATA lines are latched into the HT1632 on the rising edge of the \overline{WR} signal.
\overline{RD}	I	READ clock input with pull-high resistor. The HT1632 RAM data is clocked out on the falling edge of the \overline{RD} signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
\overline{CS}	I	Chip select input with pull-high resistor When the \overline{CS} line is high, the data and command read from or written to the HT1632 is disabled, and the serial interface circuit is also reset. If CS is low, the data and command transmission between the host controller and the HT1632 are all enabled.
LED_VSS	—	Negative power supply for driver circuit, ground.
VSS	—	Negative power supply for logic circuit, ground.
VDD	—	Positive power supply for logic and driver circuit.

Absolute Maximum Ratings

Supply Voltage $V_{SS}-0.3V$ to $V_{SS}+5.5V$ Storage Temperature $-50^{\circ}C$ to $125^{\circ}C$
 Input Voltage $V_{SS}-0.3V$ to $V_{DD}+0.3V$ Operating Temperature $-40^{\circ}C$ to $85^{\circ}C$

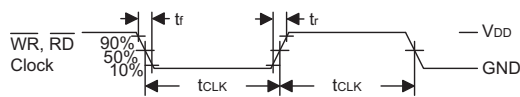
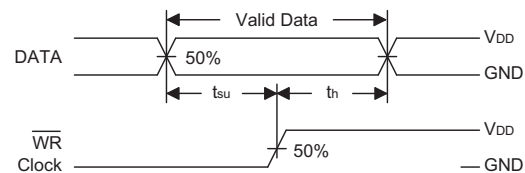
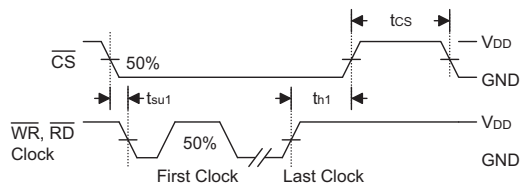
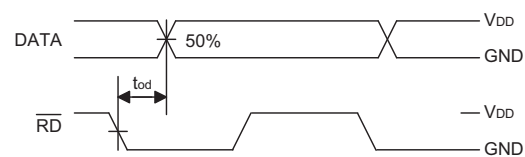
Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics
 $V_{DD}=2.4V\sim 5.5V$, $T_a=25^{\circ}C$ (Unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5.0	5.5	V
I_{DD}	Operating Current	5V	No load, LED ON, on-chip RC oscillator	—	0.3	0.6	mA
I_{STB}	Standby Current	5V	No load, power down mode	—	1.5	3.0	μA
V_{IL}	Input Low Voltage	5V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	0	—	$0.3V_{DD}$	V
V_{IH}	Input High Voltage	5V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	$0.7V_{DD}$	—	5	V
I_{OL1}	DATA	5V	$V_{OL}=0.5V$	2.5	4.0	—	mA
I_{OH1}	DATA	5V	$V_{OH}=4.5V$	-2.0	-3.5	—	mA
I_{OL2}	OSC, SYNC	5V	$V_{OL}=0.5V$	5	7	—	mA
I_{OH2}	OSC, SYNC	5V	$V_{OH}=4.5V$	-3.5	-5.0	—	mA
I_{OL3}	Common Sink Current	5V	$V_{OL}=0.5V$	100	140	—	mA
I_{OH3}	Common Source Current	5V	$V_{OH}=4.5V$	-40	-55	—	mA
I_{OL4}	LED Out Driver	5V	$V_{OL}=0.5V$	110	160	—	mA
R_{PH}	Pull-high Resistor	5V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	18	27	40	$k\Omega$

A.C. Characteristics
 $V_{DD}=2.4V\sim 5.5V, T_a=25^{\circ}C$ (Unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
f _{SYS}	System Clock	5V	On-chip RC oscillator	192	256	320	kHz
f _{LED}	LED Duty Cycle & Frame Frequency	5V	1/8 duty	—	f _{SYS} /2624	—	Hz
		5V	1/16 duty	—	f _{SYS} /2624	—	Hz
f _{CLK1}	Serial Data Clock (\overline{WR} pin)	5V	Duty cycle 50%	—	—	1	MHz
f _{CLK2}	Serial Data Clock (\overline{RD} pin)	5V	Duty cycle 50%	—	—	500	kHz
t _{CS}	Serial Interface Reset Pulse Width	—	\overline{CS}	250	—	—	ns
t _{CLK}	$\overline{WR}, \overline{RD}$ Input Pulse Width	5V	Write mode	0.5	—	—	μs
			Read mode	1.0	—	—	
t _r , t _f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	50	100	ns
t _{su}	Setup Time for DATA to $\overline{WR}, \overline{RD}$, RD Clock Width (Figure 2)	—	—	50	100	—	ns
t _h	Hold Time for DATA to $\overline{WR}, \overline{RD}$, RD, Clock Width (Figure 2)	—	—	100	200	—	ns
t _{su1}	Setup Time for \overline{CS} to $\overline{WR}, \overline{RD}$, Clock Width (Figure 3)	—	—	200	300	—	ns
t _{h1}	Hold Time for \overline{CS} to $\overline{WR}, \overline{RD}$, Clock Width (Figure 3)	—	—	100	200	—	ns
t _{od}	Data Output Delay Time (Figure 4)	—	—	—	100	200	ns


Figure 1

Figure 2

Figure 3

Figure 4

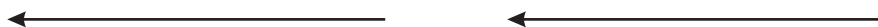
Functional Description

Display Memory – RAM

The static display memory (RAM) is organised into 64×4 bits or 96×4 bits and is used to store the display data. If 32 outbits & 8 commons is selected, the RAM size is 64×4 bits. If 24 outbits & 16 commons is selected, the RAM size is 96×4 bits. The contents of the RAM are directly mapped to the contents of the LED driver. If the

data in RAM is set to "1", the corresponding LED will be lighted. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The contents of the RAM can be read or written from bit 0 of the specific address. The following is a mapping from the RAM to the LED pattern:

	Com7	Com6	Com5	Com4	Com3	Com2	Com1	Com0		
Out0					01H				00H	
Out1					03H				02H	
Out2					05H				04H	
Out3					07H				06H	
Out4					09H				08H	
Out5					0BH				0AH	
Out6					0DH				0CH	
Out7					0FH				0EH	
Out8					11H				10H	
Out9					13H				12H	
Out10					15H				14H	
Out11					17H				16H	
Out12					19H				18H	
Out13					1BH				1AH	
Out14					1DH				1CH	
Out15					1FH				1EH	
Out16					21H				20H	
Out17					23H				22H	
Out18					25H				24H	
Out19					27H				26H	
Out20					29H				28H	
Out21					2BH				2AH	
Out22					2DH				2CH	
Out23					2FH				2EH	
Out24					31H				30H	
Out25					33H				32H	
Out26					35H				34H	
Out27					37H				36H	
Out28					39H				38H	
Out29					3BH				3AH	
Out30					3DH				3CH	
Out31					3FH				3EH	
	D3	D2	D1	D0	Addr. Data	D3	D2	D1	D0	Addr. Data



32 Outbits & 8 Common for 64×4 Display RAM

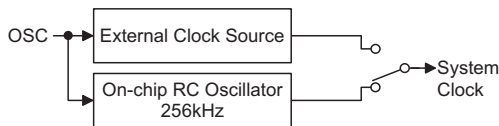
	Com15	Com14	Com13	Com12	Com3	Com2	Com1	Com0	
Out0										00H
Out1										04H
Out2										08H
Out3										0CH
Out4										10H
Out5										14H
Out6										18H
Out7										1CH
Out8										20H
Out9										24H
Out10										28H
Out11									2CH
Out12										30H
Out13										34H
Out14										38H
Out15										3CH
Out16										40H
Out17										44H
Out18										48H
Out19										4CH
Out20										50H
Out21										54H
Out22										58H
Out23									5CH
	D3	D2	D1	D0	Addr. Data	D3	D2	D1	D0	Addr. Data



24 Outbits & 16 Common for 96x4 Display RAM

System Oscillator

The HT1632 system clock is used to generate the time base clock frequency, LED-driving clock. The clock may be sourced from an on-chip RC oscillator (256kHz), or an external clock using the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LED duty cycle generator will turn off. This command is, however, available only for the on-chip RC oscillator. Once the system clock stops, the LED display will become blank, and the time base will also lose its function. The LED OFF command is used to turn the LED duty cycle generator off. After the LED duty cycle generator switches off by issuing the LED OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor execute the power down mode. The crystal oscillator option can be applied to connect an external frequency source to the OSC pin. In this case, the system fails to enter the power down mode, similar to the case in the external clock source operation. At the initial system power on, the HT1632 is in the SYS DIS state.

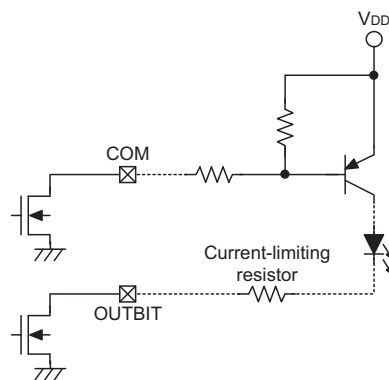


System Oscillator Configuration

LED Driver

The HT1632 has a 256 (32×8) and 384 (24×16) pattern LED driver. It can be configured in a 32×8 or 24×16 pattern and common pad N-MOS open drain output or P-MOS open drain output LED driver using the S/W configuration. This feature makes the HT1632 suitable for multiple LED applications. The LED-driving clock is derived from the system clock. The driving clock frequency is always 256kHz, an on-chip RC oscillator frequency, or an external frequency. The LED corresponding commands are summarized in the table. The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The LED OFF command turns the LED display off by disabling the LED duty cycle generator. The LED ON command, on the other hand, turns the LED display on by enabling the LED duty cycle generator.

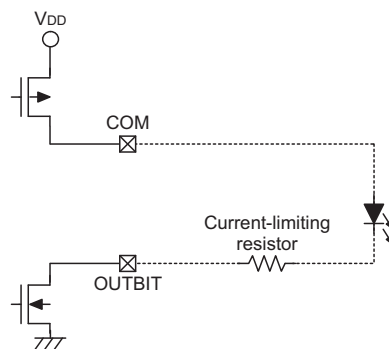
Name	Command Code	Function
LED OFF	1000000010X	Turn off LED outputs
LED ON	1000000011X	Turn on LED outputs
Commons Option	1000010abXXX	ab=00: N-MOS open drain output and 8 common option ab=01: N-MOS open drain output and 16 common option ab=10: P-MOS open drain output and 8 common option ab=11: P-MOS open drain output and 16 common option



NMOS Open Drain Driving Mode Configuration

LED Color	Current-limiting Resistor
Red	120Ω at V _{DD} =5V
Green	100Ω at V _{DD} =5V

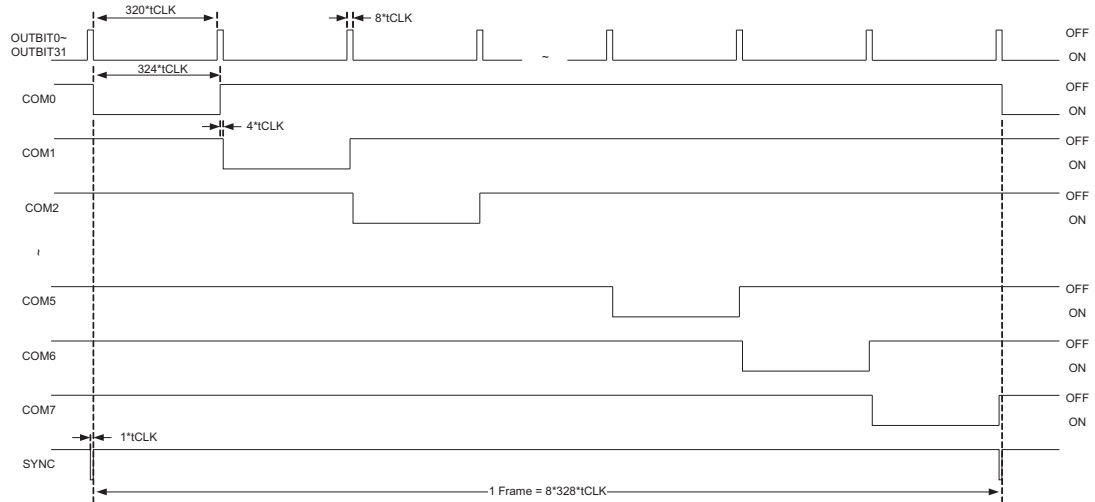
Recommended Current-limiting Resistor for NMOS Open Drain Driving Mode



PMOS Open Drain Driving Mode Configuration

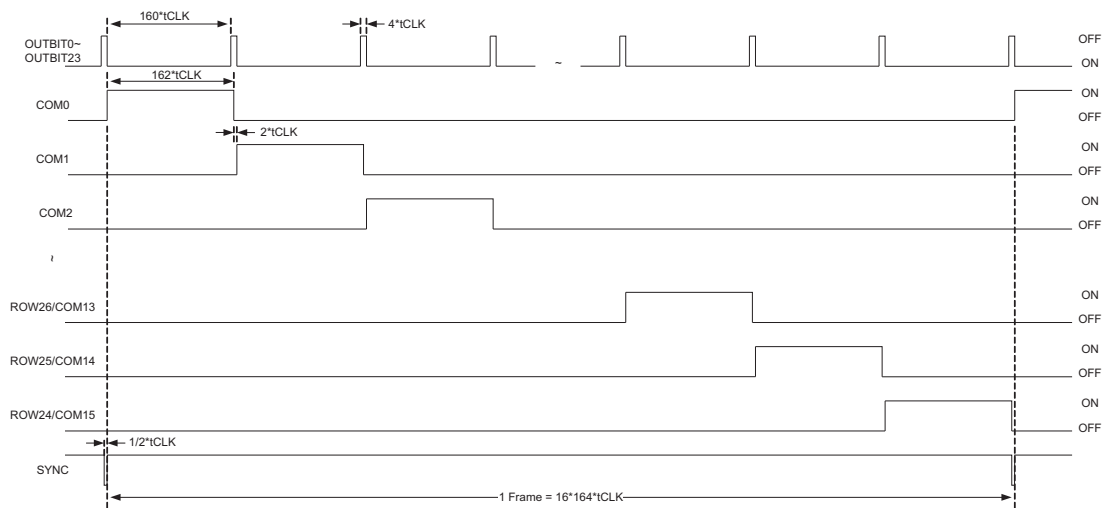
LED Driver Mode output Waveform

- N-MOS open drain of 32x8 driver mode (COM pin with transistor buffer)



Note: $t_{CLK} = 1/f_{SYS}$

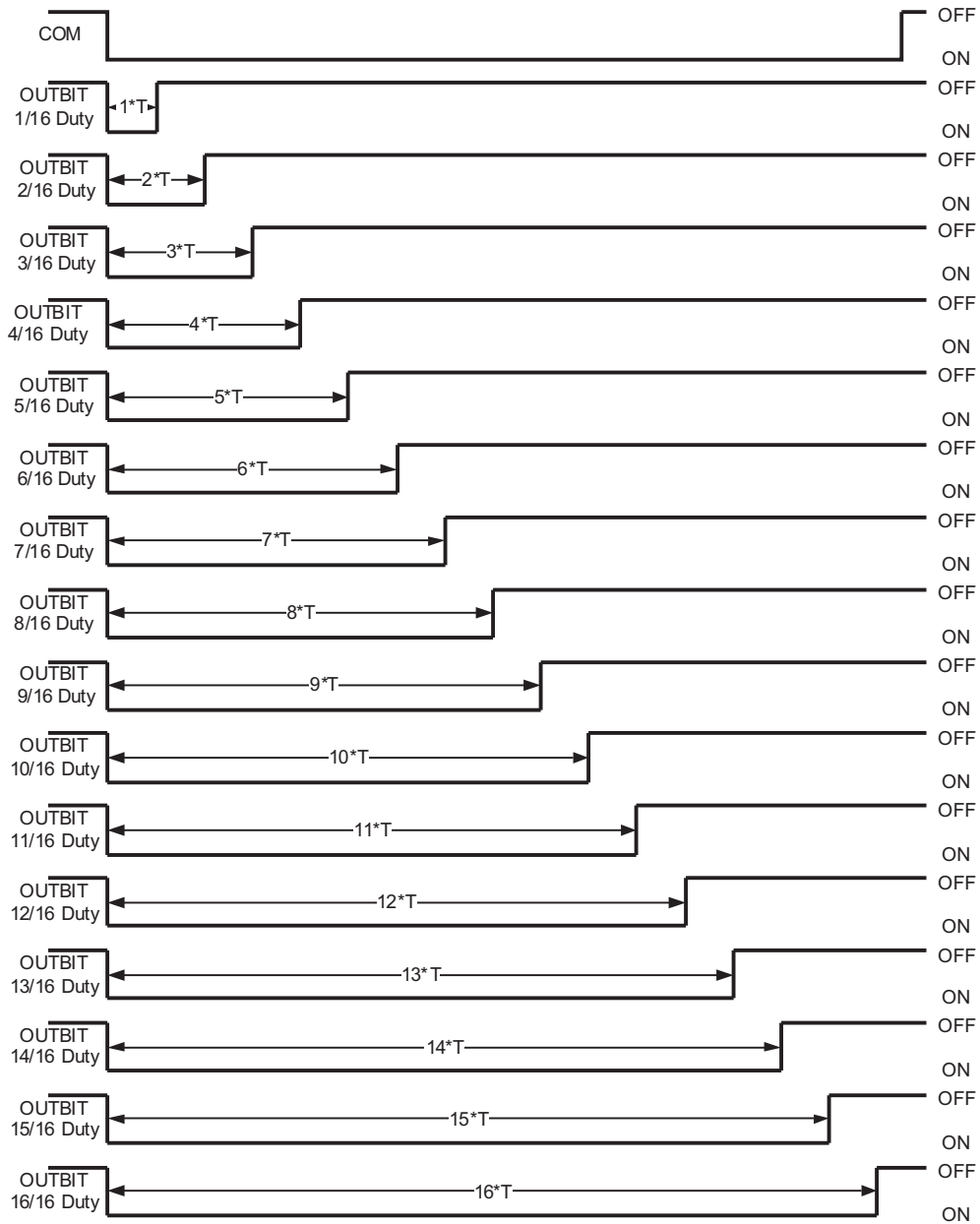
- P-MOS open drain of 24*16 driver mode



Note: $t_{CLK} = 1/f_{SYS}$

Digital Dimming

The Display Dimming capabilities of the HT1632 are very versatile. The whole display can be dimmed using pulse width modulation techniques for the OUTBIT driver with the Dimming command. The relationship between OUTBIT and COM digital dimming duty time are shown as below:



- Note:
- (1) $T=20 \times t_{CLK}$ (32x8 driver mode)
 - (2) $T=10 \times t_{CLK}$ (24x16 driver mode)
 - (3) $t_{CLK}=1/f_{SYS}$

Cascade operation

For the cascade operation, the first IC is set to master mode and its SYNC and OSC pins are set to output pins. The second IC is set to slave mode and its SYNC and OSC pins are set to input pins which are connected to the the master IC. Please refer to the "Cascade control flow chart" for detail settings.

Blinker

The HT1632 has display blinking capabilities. The blink function generates all LED blinking. The blink rates is 0.25s LED on and 0.25s LED off for one blinking period. This blinking function can be effectively performed by setting the BLINK ON or BLINK OFF command.

Command Format

The S/W setting can configure the HT1632. There are two mode commands to configure the HT1632 resources and to transfer the LED display data. The configuration mode of the HT1632 is knows as the command mode,with a command mode ID of 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LED configuration command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

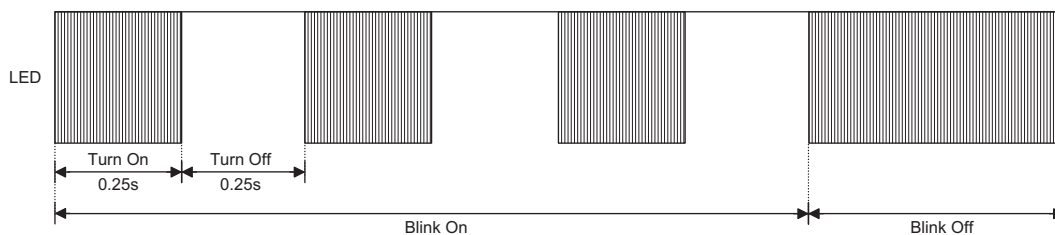
The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the \overline{CS} pin should be set to "1" and the previous operation mode will be reset also. Once the \overline{CS} pin returns to "0", a new operation mode ID should be issued first.

Interfacing

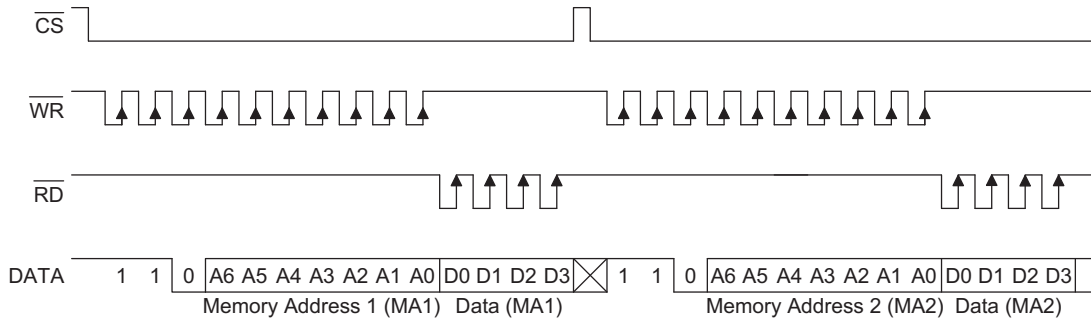
Only four lines are required to interface to the HT1632. The \overline{CS} line is used to initialise the serial interface circuit and to terminate the communication between the host controller and the HT1632. If the \overline{CS} pin is set to 1, the data and command issued between the host controller and the HT1632 are first disabled and then initialised. Before issuing a mode command or mode switching, a high level pulse is required to initialise the serial interface of the HT1632. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The \overline{RD} line is the READ clock input. Data in the RAM is clocked out on the falling edge of the \overline{RD} signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller reads in the correct data during the interval between the rising edge and the next falling edge of the \overline{RD} signal. The \overline{WR} line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1632 on the rising edge of the \overline{WR} signal.



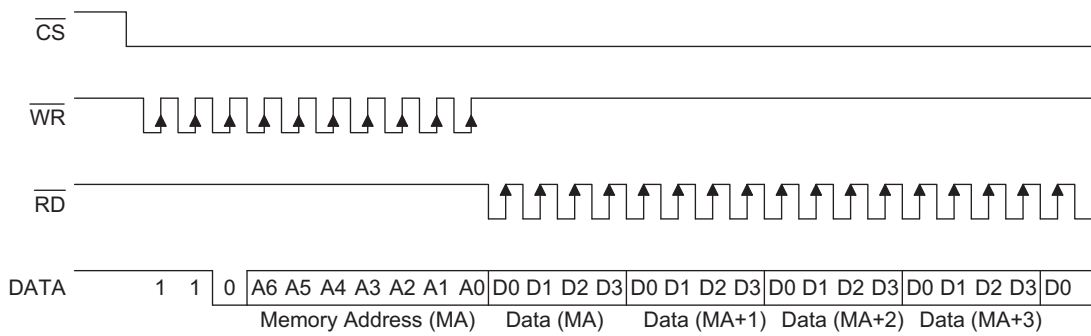
Example of Waveform for Blinker

Timing Diagrams

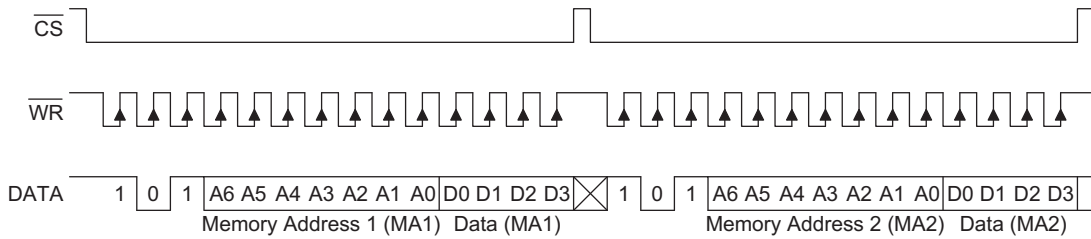
READ Mode – Command Code = 1 1 0



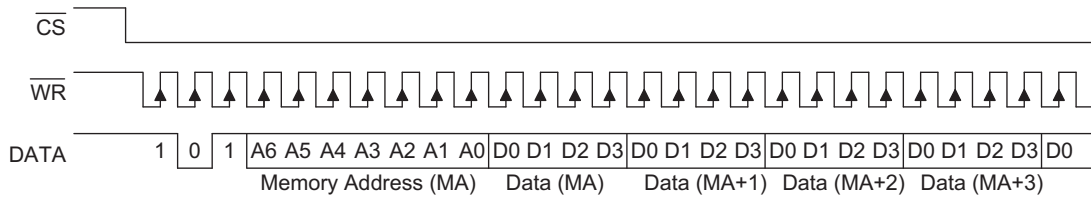
READ Mode – Successive Address Reading



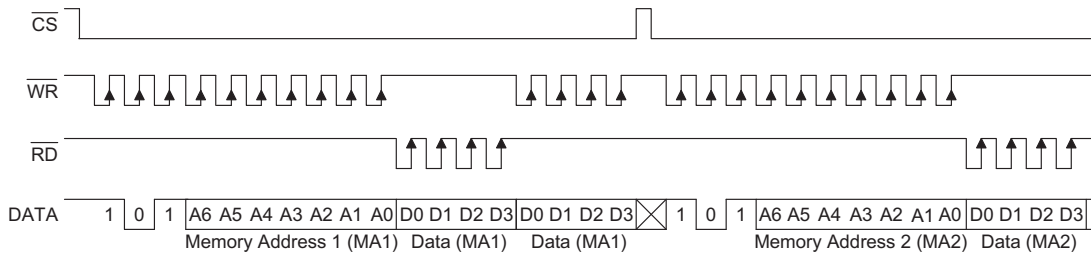
WRITE Mode – Command Code = 1 0 1



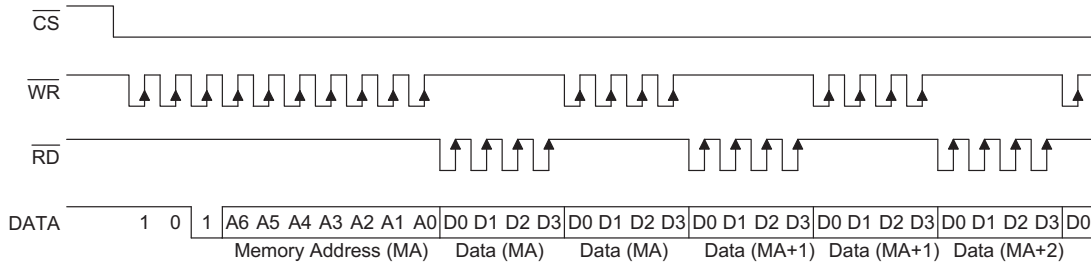
WRITE Mode – Successive Address Writing



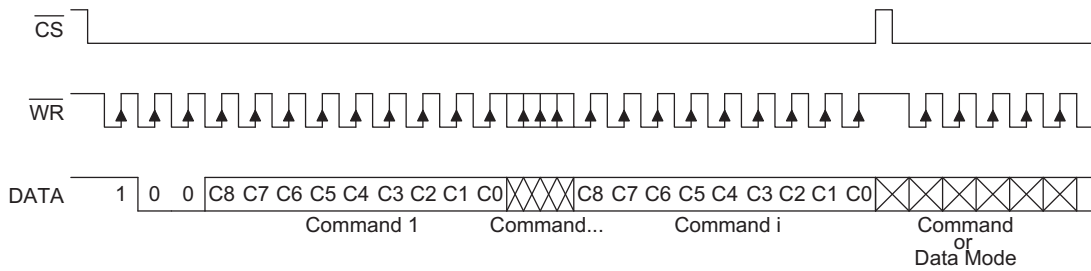
READ-MODIFY-WRITE Mode – Command Code = 1 0 1



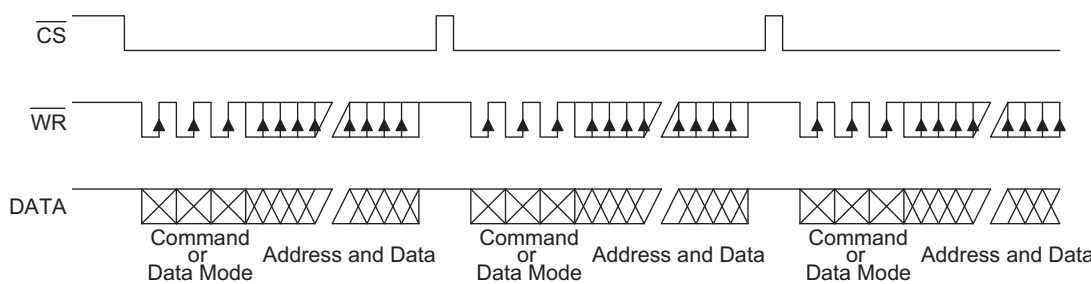
READ-MODIFY-WRITE Mode – Successive Address Accessing



Command Mode – Command Code = 1 0 0

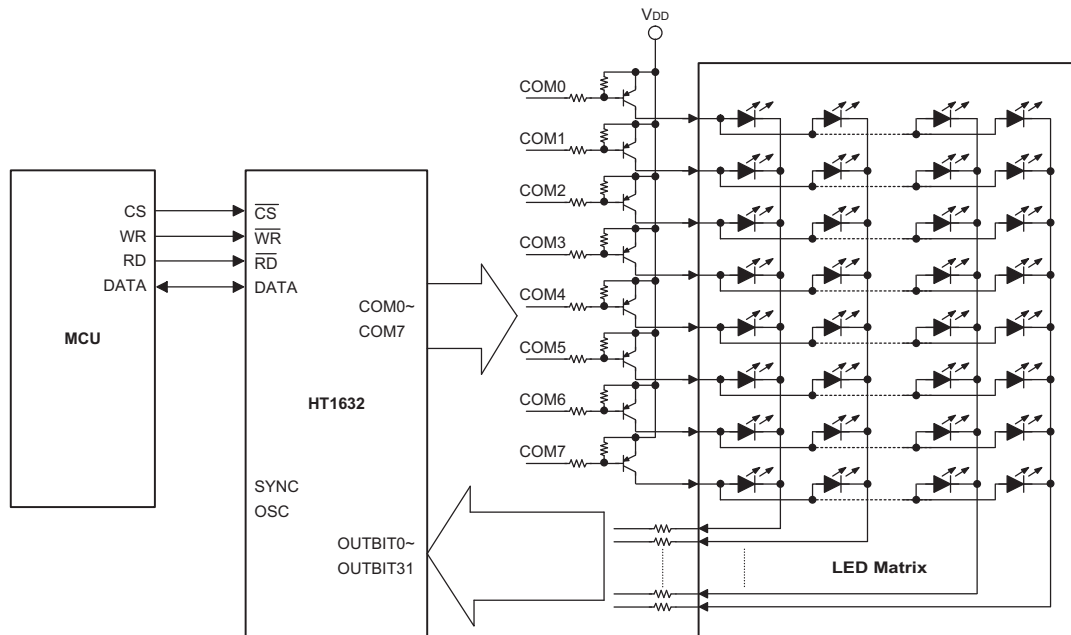


Mode – Data and Command Mode



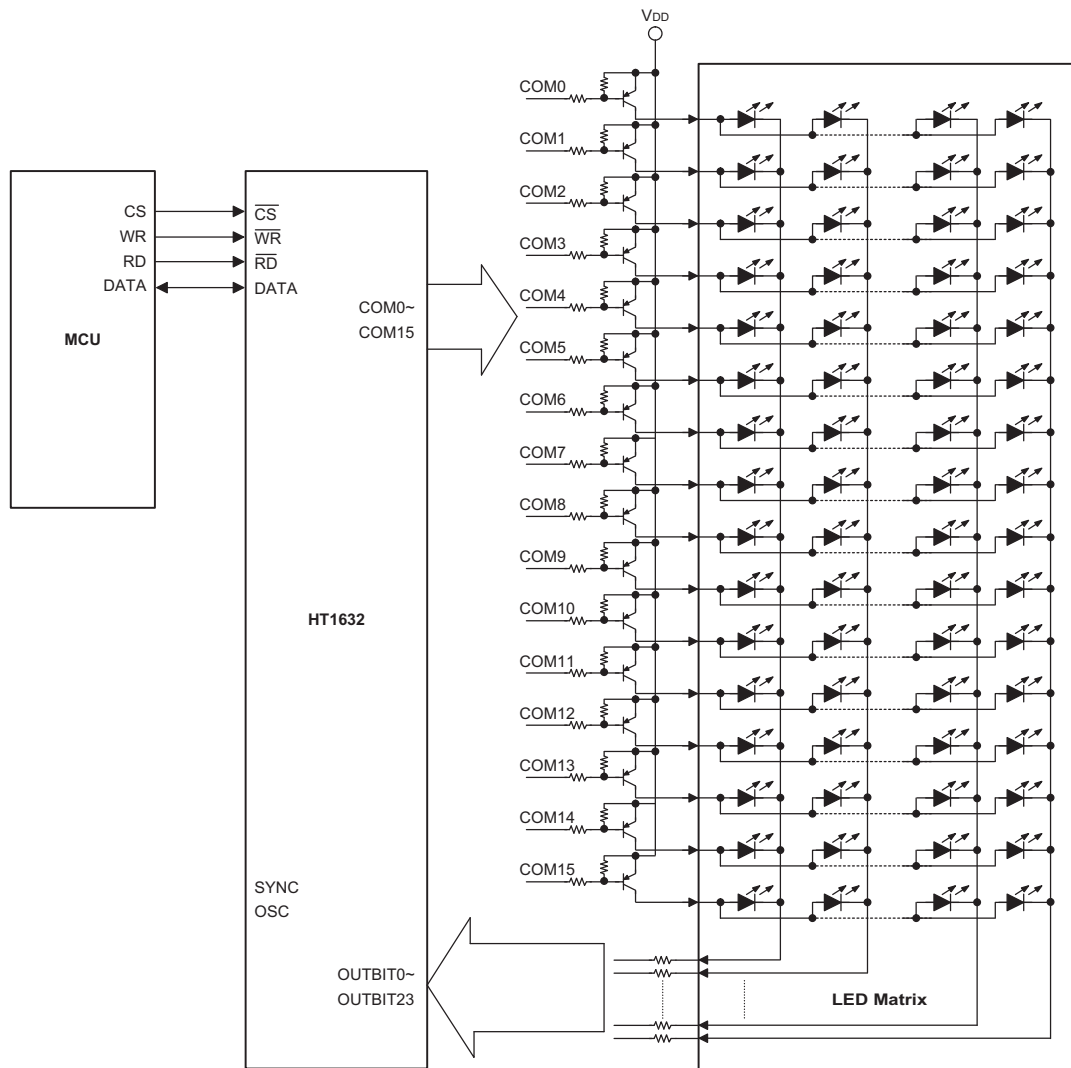
Application Circuits

Single Connect Example for 32 Outbits & 8 Commons (NMOS)



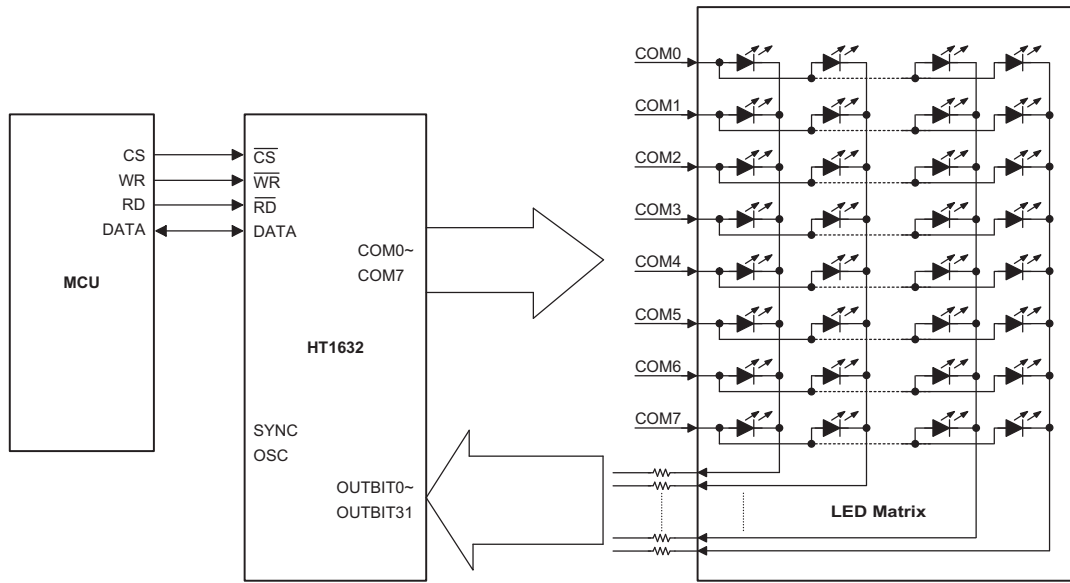
Note: Common & outbit are all NMOS open drain output structures and only supply sink current.

Single Connect Example for 24 Outbits & 16 Commons (NMOS)



Note: Common & outbit are all NMOS open drain output structures and only supply sink current.

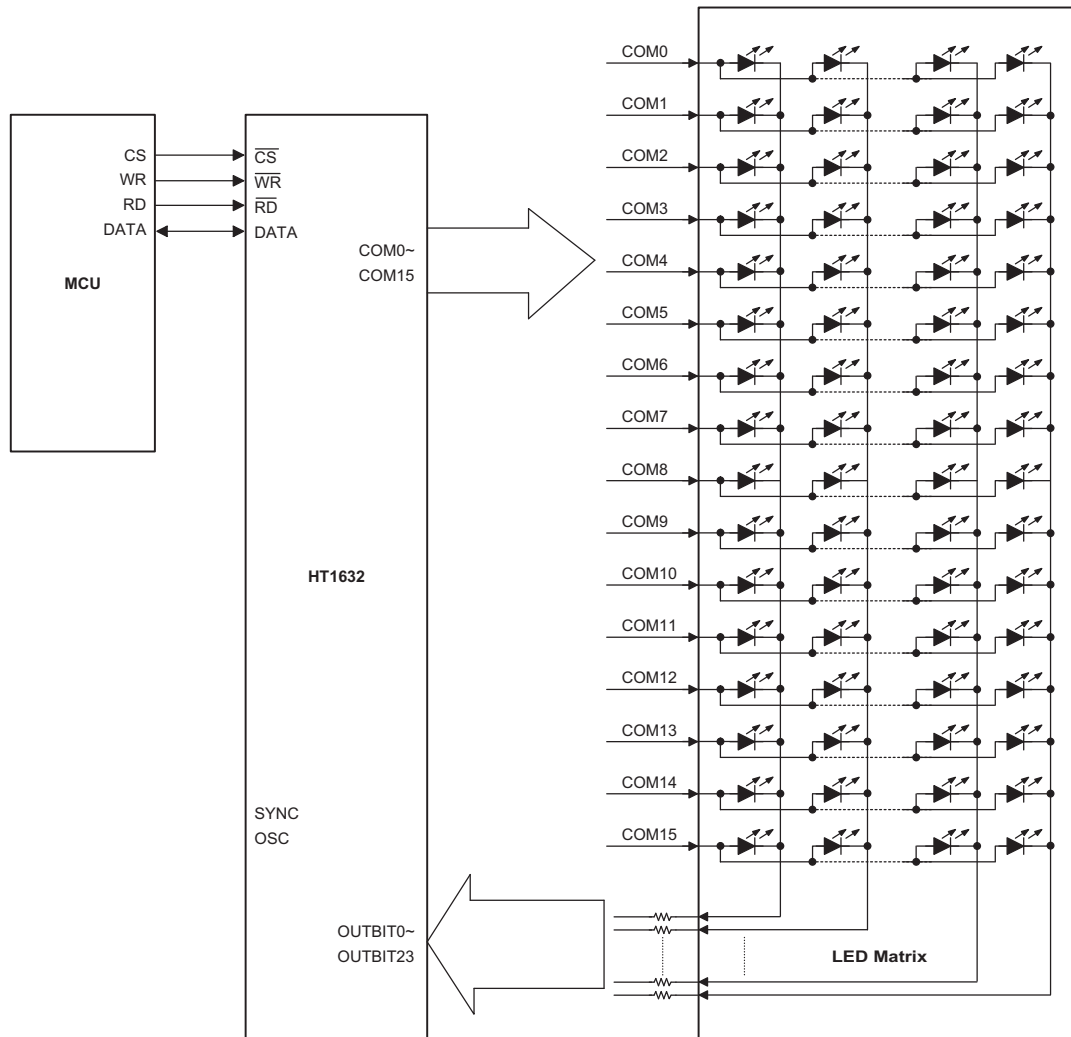
Single Connect Example for 32 Outputs & 8 Commons (PMOS)



Note: Outbit are NMOS open drain output structures and only supply sink current, common are PMOS open drain output structures and only supply source current.

If the P-MOS open drain structure is used for the commons, the brightness of the LEDs may be not enough and the uniformity of the LEDs may be not good. If user cares about the brightness and uniformity of the LEDs, the N-MOS open drain structure is suggested being used for the commons.

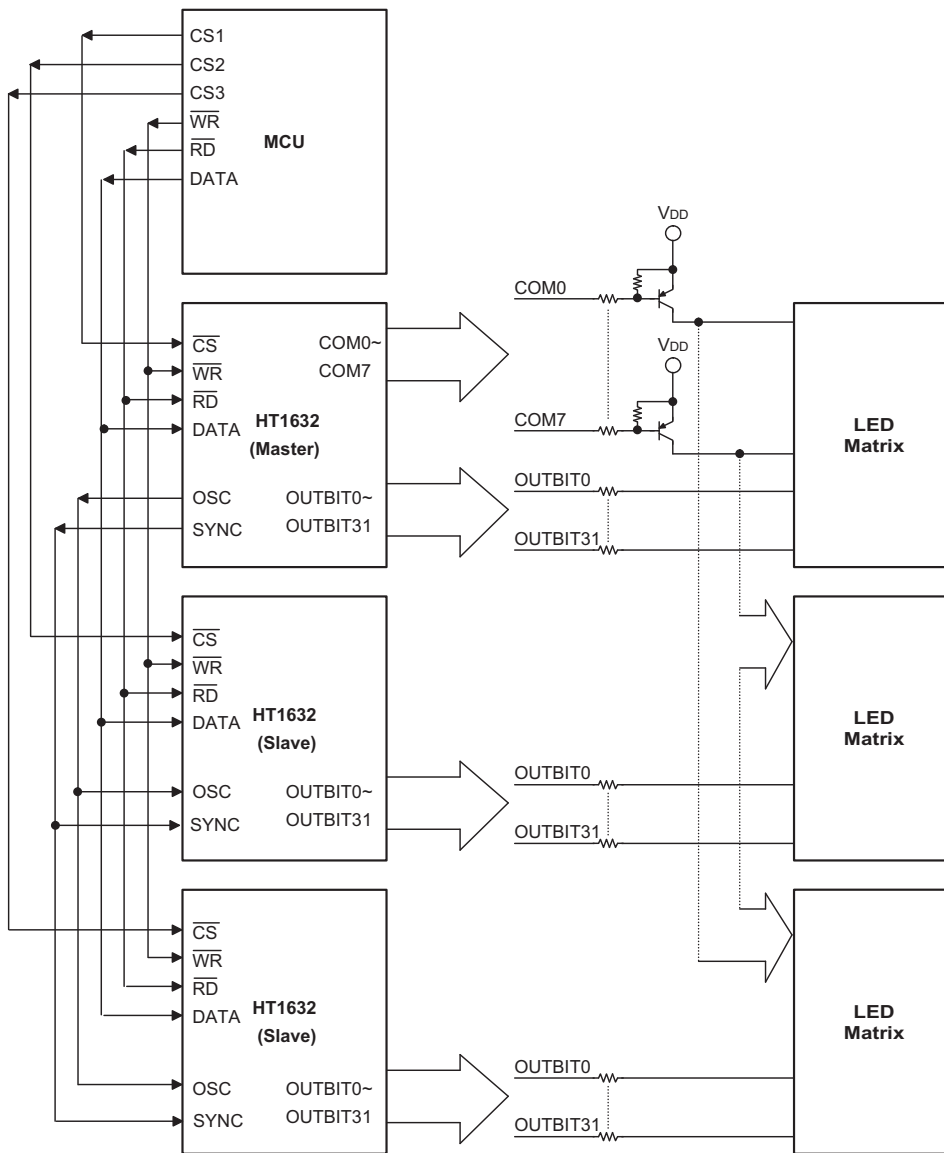
Single Connect Example for 24 Outbits & 16 Commons (PMOS)



Note: Outbit are NMOS open drain output structures and only supply sink current, common are PMOS open drain output structures and only supply source current.

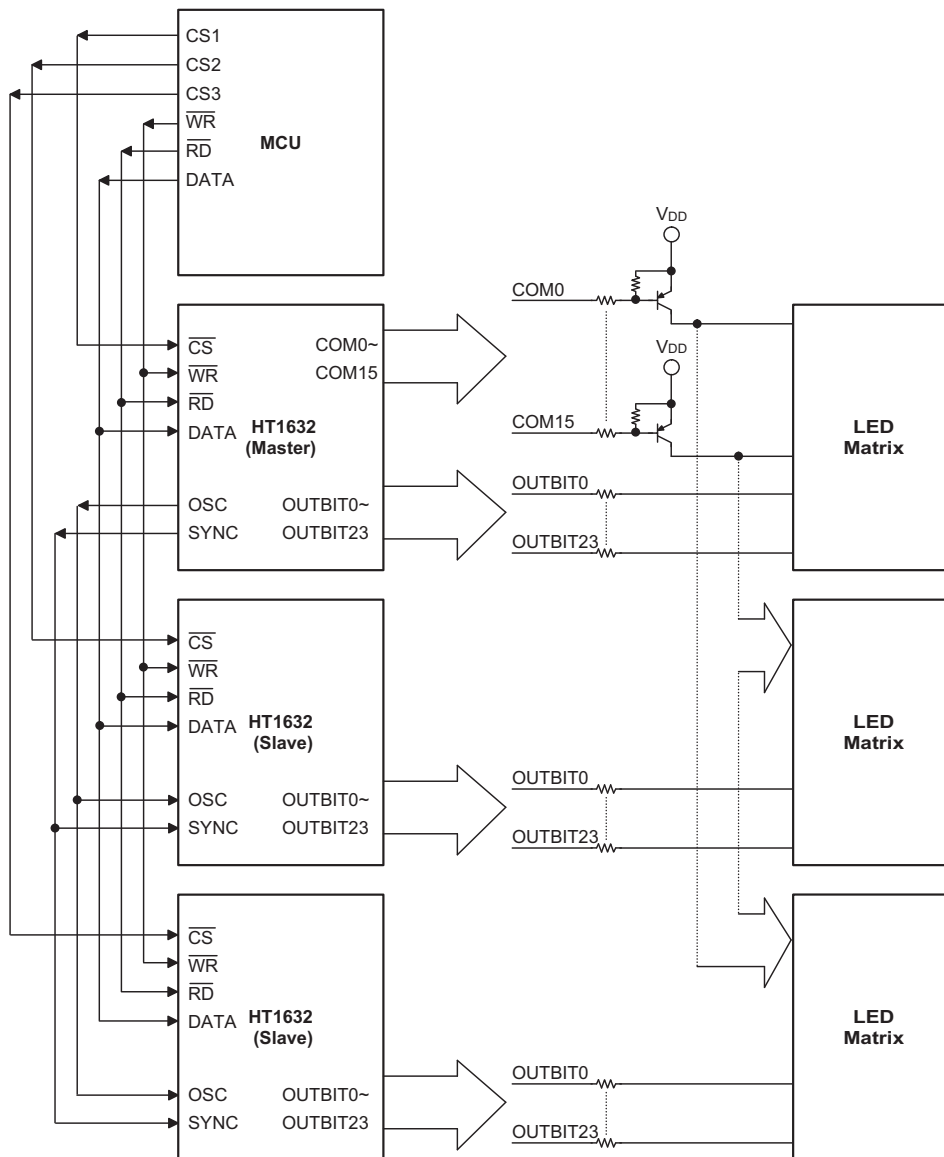
If the P-MOS open drain structure is used for the commons, the brightness of the LEDs may be not enough and the uniformity of the LEDs may be not good. If user cares about the brightness and uniformity of the LEDs, the N-MOS open drain structure is suggested being used for the commons.

Cascade Connect Example for 32 Outbits & 8 Commons



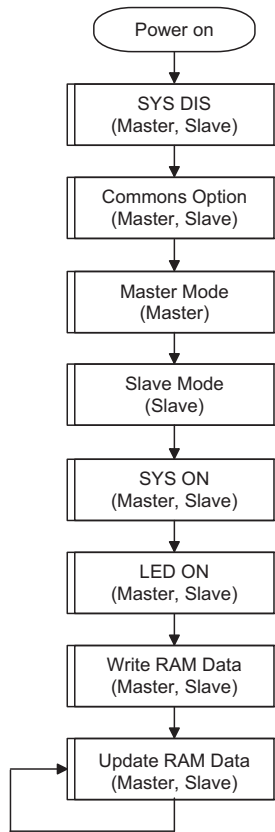
Note: It also can set cascade mode by software. User must set the Slaves in external clock mode with command. The CS pin must be connected to MCU individually for independent read-write.

Cascade Connect Example for 24 Outbits & 16 Commons



Note: It also can set cascade mode by software. User must set the Slaves in external clock mode with command. The CS pin must be connected to MCU individually for independent read-write.

Cascade Control Flow



Command Summary

Name	ID	Command Code	D/C	Function	Default
READ	1 1 0	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LED duty cycle generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LED OFF	1 0 0	0000-0010-X	C	Turn off LED duty cycle generator	Yes
LED ON	1 0 0	0000-0011-X	C	Turn on LED duty cycle generator	
BLINK OFF	1 0 0	0000-1000-X	C	Turn off blinking function	Yes
BLINK ON	1 0 0	0000-1001-X	C	Turn on blinking function	
SLAVE MODE	1 0 0	0001-00XX-X		Set slave mode and clock source from external clock	
MASTER MODE	1 0 0	0001-01XX-X		Set master mode and clock source on-chip RC oscillator, the system clock output to OSC pin	
RC	1 0 0	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT CLK	1 0 0	0001-11XX-X	C	System clock source, external clock source	
COMMONS OPTION	1 0 0	0010-abXX-X	C	ab=00: N-MOS open drain output and 8 common option ab=01: N-MOS open drain output and 16 common option ab=10: P-MOS open drain output and 8 common option ab=11: P-MOS open drain output and 16 common option	ab =10
PWM Duty	1 0 0	101X-0000-X	C	PWM 1/16 duty	
	1 0 0	101X-0001-X	C	PWM 2/16 duty	
	1 0 0	101X-0010-X	C	PWM 3/16 duty	
	1 0 0	101X-0011-X	C	PWM 4/16 duty	
	1 0 0	101X-0100-X	C	PWM 5/16 duty	
	1 0 0	101X-0101-X	C	PWM 6/16 duty	
	1 0 0	101X-0110-X	C	PWM 7/16 duty	
	1 0 0	101X-0111-X	C	PWM 8/16 duty	
	1 0 0	101X-1000-X	C	PWM 9/16 duty	
	1 0 0	101X-1001-X	C	PWM 10/16 duty	
	1 0 0	101X-1010-X	C	PWM 11/16 duty	
	1 0 0	101X-1011-X	C	PWM 12/16 duty	
	1 0 0	101X-1100-X	C	PWM 13/16 duty	
	1 0 0	101X-1101-X	C	PWM 14/16 duty	
	1 0 0	101X-1110-X	C	PWM 15/16 duty	
	1 0 0	101X-1111-X	C	PWM 16/16 duty	Yes

Note: X: Don't care

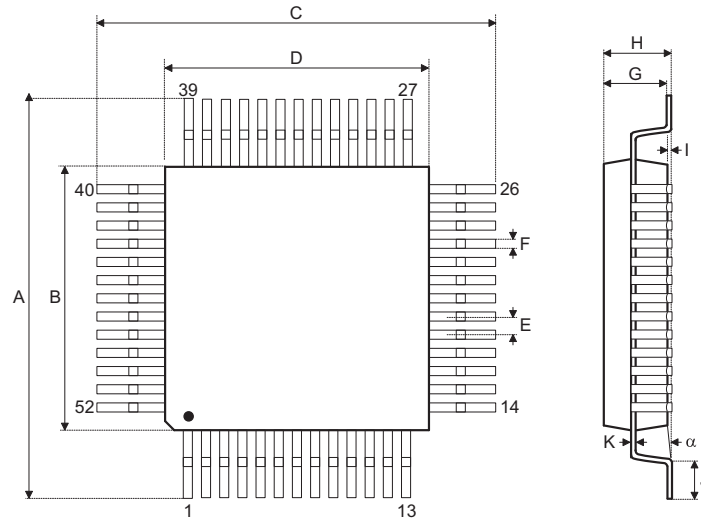
A6~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

Default: Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Among these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base clock frequency can be derived from an on-chip RC oscillator or an external clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1632 after power on reset, for power on reset may fail, which in turn leads to the malfunction of the HT1632

Package Information
52-pin QFP (14mm×14mm) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.681	—	0.689
B	0.547	—	0.555
C	0.681	—	0.689
D	0.547	—	0.555
E	—	0.039	—
F	—	0.016	—
G	0.098	—	0.122
H	—	—	0.134
I	—	0.004	—
J	0.029	—	0.041
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	17.30	—	17.50
B	13.90	—	14.10
C	17.30	—	17.50
D	13.90	—	14.10
E	—	1.00	—
F	—	0.40	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	0.73	—	1.03
K	0.10	—	0.20
α	0°	—	7°

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